ATA5008
DigiSensor™
V2.1

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Overview

The ATA5008 focuses on reducing power consumption, improving immunity against various internal and external noises and achieving tuning free applications. It also includes a hardwired position calculator to find one dimensional or two dimensional interpolated coordinates.

The ATA5008 uses time-domain multiplexing (TDM) architecture to measure capacitance variations of input channels and uses an optimized internal voltage regulator with a smart power management scheme in order to significantly reduce power consumption. The ATA5008 also adopts active pulse-pass architecture to improve noise immunity to achieve better performance in noisy environments. Its widened dynamic range which compensates for parasitic capacitance in the sensing channel eliminates troublesome hardware tuning. A tuning-free development eventually shortens the development period by reducing PCB design iterations.

In addition to these major changes in technology, the ATA5008 has several new features such as 1D/2D interpolation and configurable general-purpose output channels. With a limited number of input channels the ATA5008 is able to calculate interpolated coordinates of up to Max.6000 times per second. The ATA5008 has a total of 21 channels, and each of which can be configured to be either a sensor input or a general-purpose output. All the previously existing functions such as APIS, AIC, FILTER, and upgraded 10-bit capacitance data, etc. still remain in the ATA5008.

The ATA5008 comes with two package types: 32-pin QFN and 24-pin QFN.

In addition to QFN packages, 64-pin FBGA package was recently added in the ATA5008 family. 64-pin FBGA package where two ATA5008 dies are bonded to support 42 sensor inputs is specially designed for the pure multi-touch screen panel using single layer sensor sheet for smart phones or hand held devices having up to 3 inch display. Using single layer sensor sheet with ATLab proprietary patterns gives customers many benefits such as higher transparency, lower cost of sensor sheet, and even higher production ratio in assembly.

Features

- Patented Pulse-Pass TDM architecture
- 21 channels configurable to be either sensor inputs or general-purpose outputs
- Current driving capability for general-purpose outputs: 14mA sink current and 8mA source current at VDDH 3.3V
- Two types of interrupts: TINT with level trigger and GINT
- Wakeup from IDLE power saving state by touch operation
- Programmable registers to characterize applications
- I^2C and SPI interfaces with the host MCU
- Configurable AIC™ (Automatic Impedance Calibration)
- Two different modes for APIS™ (Adjacent Pattern Interference Suppression)
- Two stage digital filter blocks are included
- Position calculator to generate 1D or 2D interpolated coordinates

Applications

- Portable devices such as PDAs, cellular phones, MP3 players, remote controllers, and other integrated input devices
- Home appliances and consumer electronic products
- Computer input devices such as mice and keyboards, Touch PAD

Ordering Information

Product Code	Package Type	Package Dimension	Pin Pitch	Num. of Sensor Inputs or Num. of Digital Outputs
ATA5008DA-32N	32-pin QFN	4mm x 4mm x 0.55mm	0.4mm	21
ATA5008DA-24N	24-pin QFN	4mm x 4mm x 0.55mm	0.5mm	13
ATA5008DA-24S	24-pin SSOP	8.2mm x 7.8mm x 2mm	0.65mm	13
ATA5008DA-64B	64-pin BGA	6mm x 6mm x 1.2mm	0.65mm	42

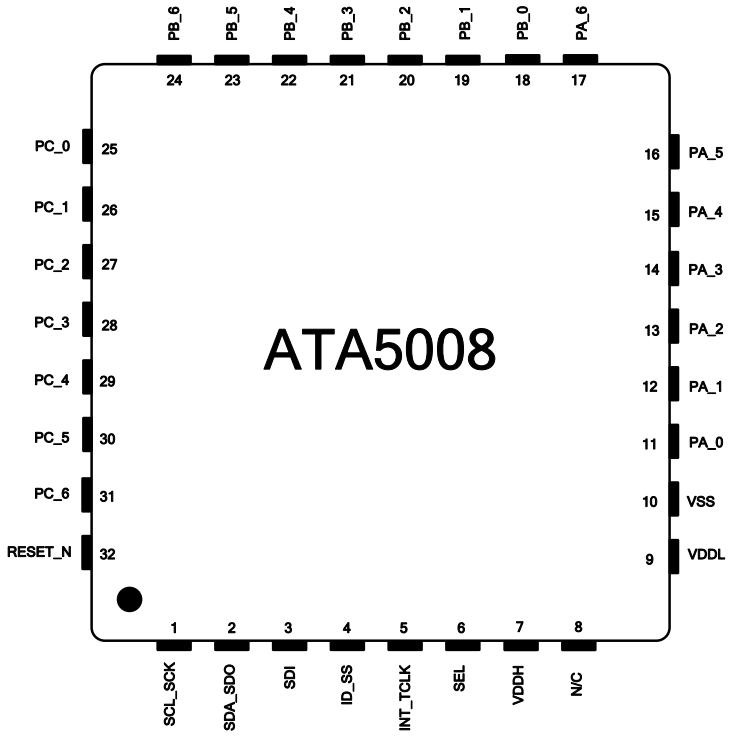

Fig. 1 ATA5008DA-32N Package

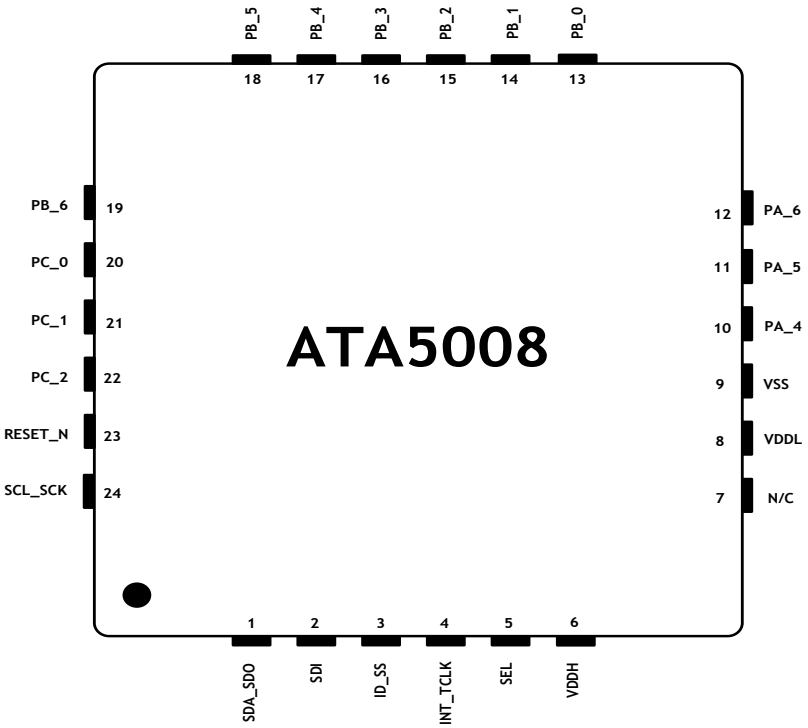

Fig. 2 ATA5008DA-24N Package

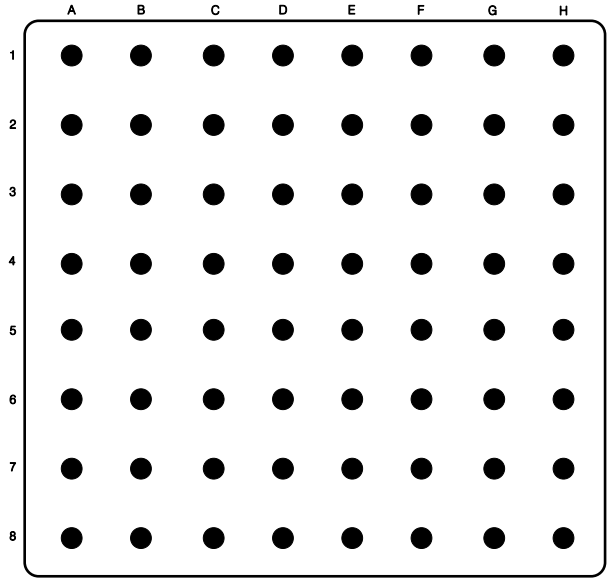

Fig. 3 ATA5008DA-64B Package

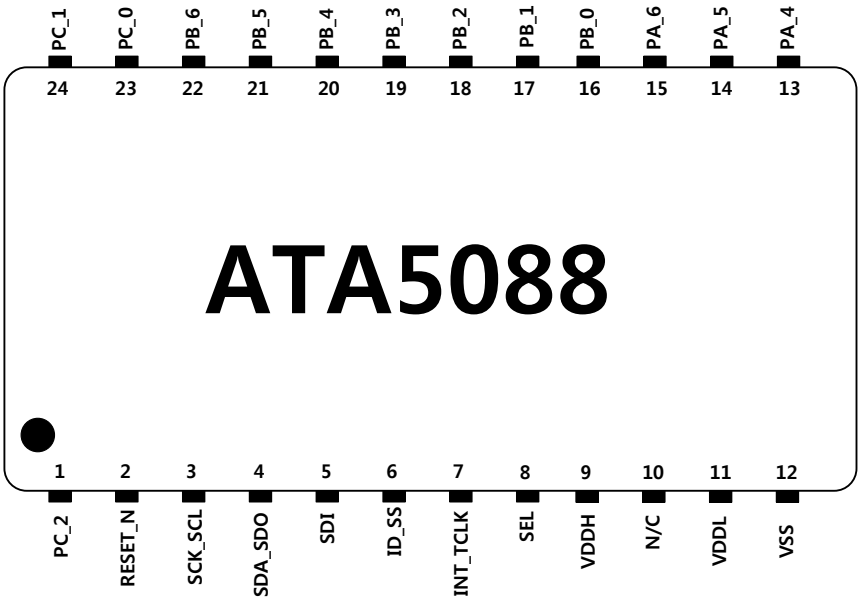

Fig. 3 ATA5008DA-64B Package

Electrical Specifications

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
	ABSOLUTE MAXIMUM RATINGS					
Tstg	Storage Temperature		-40		90	℃
Topr	Operating Temperature		-35		85	℃
VDDH	IO Power Supply Voltage		1.6	3.3	5.5	V
VDDL	Core Power Supply Voltage		1.65	1.8	1.95	V
ESD	HBM			±5		KV
	MM			±200		V
	RECOMMENDED OPERATING CONDITIONS					
Toprr	Operating Temperature		-30	25	80	℃
Vddp	Power Supply Voltage (VDDH)		1.65		4.0	V
Vddc	Power Supply Voltage (VDDL)		1.7	1.8	1.9	V
Tr_i	Digital Input Rising Time	Input Pin			5	ns
Tf_i	Digital Input Falling Time	Input Pin			5	ns
	AC ELECTRICAL SPECIFICATIONS (Typical values at Ta=25℃ and VDDH=3.3V)					
fsys	System Clock		1.8	2	2.2	MHz
fs	Touch Input sampling frequency	When System Clock is 2MHz	3.4		12	KHz
Dr_c	Coordinate output Data Rate	When System Clock is 2MHz, maximum fs	24	200	6000	Hz
Dr_t	Touch output Data Rate	When System Clock is 2MHz	34		120	Hz
Stch	Touch Sensitivity		2.2	5.5	16.8	fF
Rs_i	Sensor Input Resistance		10	34	90	KΩ
Coff	Allowable Offset Capacitance for Channel to GND	When Max Rs_i = 34K ohm	136	170	204	pF
Tr_o	Output Rising Time	Load = 100pF		50	60	ns
Tf_o	Output Falling Time	Load = 100pF		50	60	ns
	DC ELECTRICAL SPECIFICATIONS (Typical values at Ta=25℃, VDDH=3.3V and VDDH = 1.8V)					
Idd_ae	Supply Current (Active mode)	When using 1.8V VDDL, Fs = 3.4Khz, *Note*: 64-pin FBGA consumes supply current twice.*	70 (140*)	115 (230*)	170 (340*)	µA
Idd_ie	Supply Current (Idle mode)			40 (80*)		µA
Idd_se	Supply Current (Sleep mode)			30 (60*)		µA
Vil	Digital Input Low Voltage				0.25xVDDH	V
Vih	Digital Input High Voltage		0.7xVDDH			V
Vol	Digital Output Low Voltage	When VDDH=3.3V Isink = 14mA When VDDH=1.8V Isink = 2mA	0.15xVDDH			V
Voh	Digital Output High Voltage	When VDDH=3.3V,Isource = 8mA When VDDH=1.8V,Isource = 2mA			0.8 x VDDH	V
Idrsnk	GPO, I2C, INT Driving(Sinl Current	VDDH=3.3V	- 14			mA
		VDDH =1.8V	- 2			mA
Idrsrc	GPO, I2C, INT Driving (Source Current	VDDH=3.3V			8	mA
		VDDH =1.8V			2	mA

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Pin Description

32QFN

Pin No.	Name	I/O	Description
32	RESET_N	I	Reset, active LOW
5	INT/TCLK	IO	O: Interrupt Output (default), I: Test Clock Input
6	SEL	I	Host Communication Selection: I^2C(L), SPI(H)
11..17	PA	IO	7 Ports for Sensor Input or GPO
18..24	PB	IO	7 Ports for Sensor Input or GPO
25..31	PC	IO	7 Ports for Sensor Input or GPO
2	SDA/SDO	IO	Bi-directional I^2C Data from/to the Host MCU or SPI Data out to Host MCU
1	SCL/SCK	I	I^2C CLK or SPI CLK from Host MCU
3	SDI	I	SPI Data input from Host MCU
4	ID/SS	I	I2C ID selection pin or SPI Slave Select from Host MCU
7	VDDH	P	IO Power (1.8V, 3.3V or 5.0V)
8	N/C	-	-
9	VDDL	P	1.8V Core Power
10	VSS	P	Ground

24QFN

Pin No.	Name	I/O	Description
23	RESET_N	I	Reset, active LOW
4	INT/TCLK	IO	O: Interrupt Output (default), I: Test Clock Input
5	SEL	I	Host Communication Selection: I^2C(L), SPI(H)
10..12	PA	IO	3 Ports for Sensor Input or GPO
13..19	PB	IO	7 Ports for Sensor Input or GPO
20..22	PC	IO	3 Ports for Sensor Input or GPO
1	SDA/SDO	IO	Bi-directional I^2C Data from/to the Host MCU or SPI Data out to Host MCU
24	SCL/SCK	I	I^2C CLK or SPI CLK from Host MCU
2	SDI	I	SPI Data input from Host MCU
3	ID/SS	I	I2C ID selection pin or SPI Slave Select from Host MCU
6	VDDH	P	IO Power (1.8V, 3.3V or 5.0V)
7	N/C	-	-
8	VDDL	P	1.8V Core Power
9	VSS	P	Ground

64FBGA

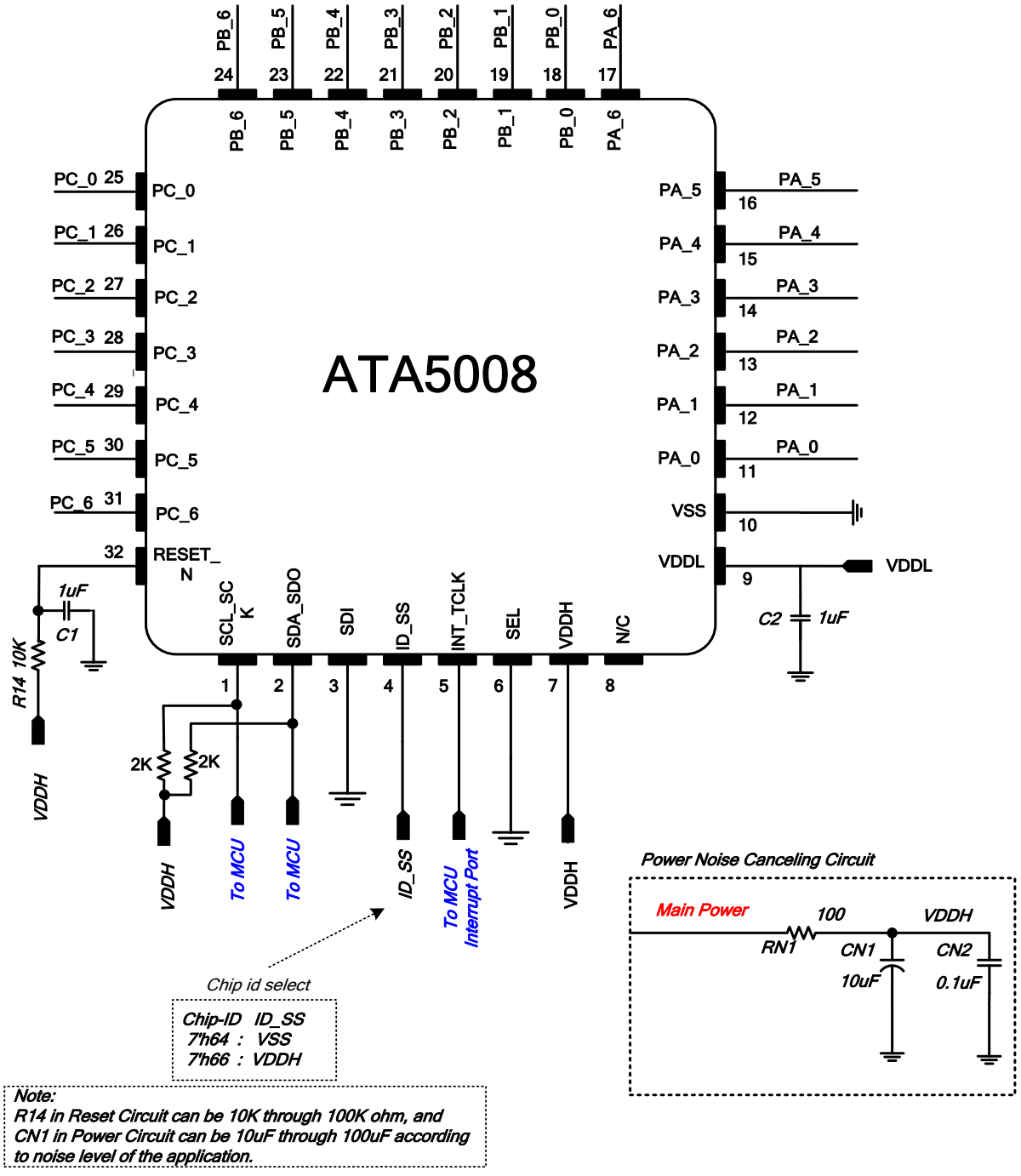
Pin number	Name	Width	IO	Description
A2, H7	BRESET_N, ARESET_N	1	I	Reset, active LOW
D6, E3	BINT_TCLK, AINT_TCLK	1	IO	Interrupt Output or Test Clock Input
D4, E5	ASEL, BSEL	1	I	Host Communication: I^2C or SPI
B1, C1, C2, D1, D2, E1, E2	APA	7	IO	7 Ports for Sensor Input or GPO
D7,D8,E7,E8,F7,F8,G8	BPA	7	IO	7 Ports for Sensor Input or GPO
F1..F3, G1,G2, H1, H2	APB	7	IO	7 Ports for Sensor Input or GPO
A7,A8,B7,B8,C6..C8	BPB	7	IO	7 Ports for Sensor Input or GPO
G3..G5,H3..H6	APC	7	IO	7 Ports for Sensor Input or GPO
A3..A6,B4..B6	BPC	7	IO	7 Ports for Sensor Input or GPO
B3, G6	BSCL_SCK, ASCL_SCK	1	I	I^2C CLK or SPI CLK from the Host MCU
C4, F5	BSDA_SDO, ASDA_SDO	1	IO	Bi-directional I^2C Data from/to the Host MCU or SPI Data out to Host MCU
C5, F4	BSDI, ASDI	1	I	SPI Data input from Host MCU
D5, E4	BID_SS, AID_SS	1	I	I^2C Chip ID setting or SPI Slave Select from Host MCU
D3, E6	AVDDH, BVDDH	1	P	IO power (1.8V, 3.3V, or 5.0V)
C3, F6	N/C	-	-	-
B2, G7	AVDDL, BVDDL	1	P	1.8V Core Power
A1, H8	AVSS, BVSS	1	P	Ground

24SSOP

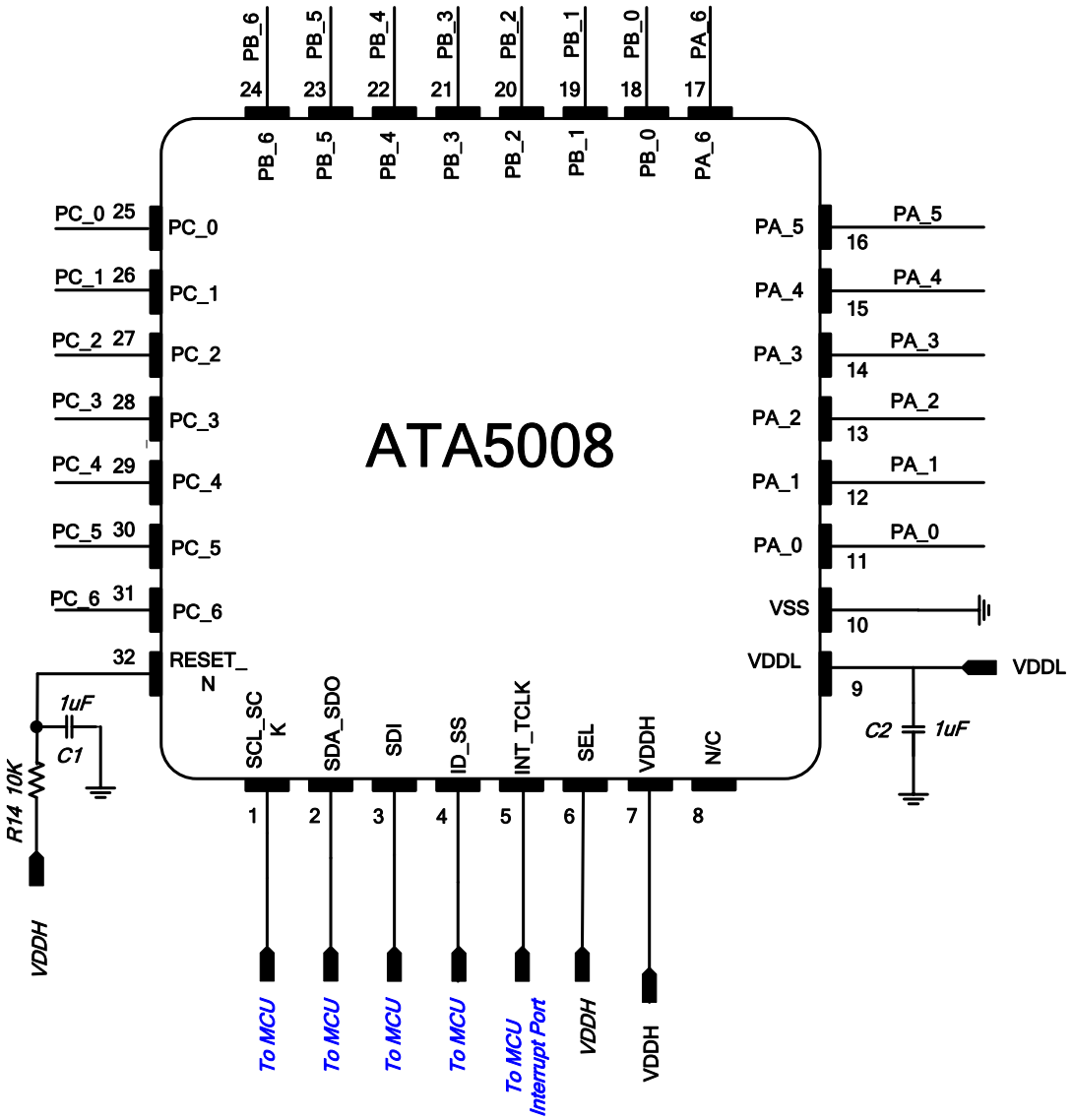
Pin No.	Name	I/O	Description
2	RESET_N	I	Reset, active LOW
7	INT/TCLK	IO	O: Interrupt Output (default), I: Test Clock Input
8	SEL	I	Host Communication Selection: I^2C(L), SPI(H)
13..15	PA	IO	3 Ports for Sensor Input or GPO
16..22	PB	IO	7 Ports for Sensor Input or GPO
23,24,1	PC	IO	3 Ports for Sensor Input or GPO
4	SDA/SDO	IO	Bi-directional I^2C Data from/to the Host MCU or SPI Data out to Host MCU
3	SCL/SCK	I	I^2C CLK or SPI CLK from Host MCU
5	SDI	I	SPI Data input from Host MCU
6	ID/SS	I	I2C ID selection pin or SPI Slave Select from Host MCU
9	VDDH	P	IO Power (1.8V, 3.3V or 5.0V)
10	N/C	-	-
11	VDDL	P	1.8V Core Power
12	VSS	P	Ground

Application Circuit

32QFN Application Circuit – I²C Interface

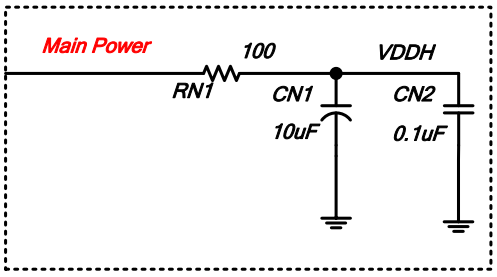


32QFN Application Circuit – SPI Interface



Note:
R14 in Reset Circuit can be 10K through 100K ohm, and CN1 in Power Circuit can be 10uF through 100uF according to noise level of the application.

Power Noise Canceling Circuit



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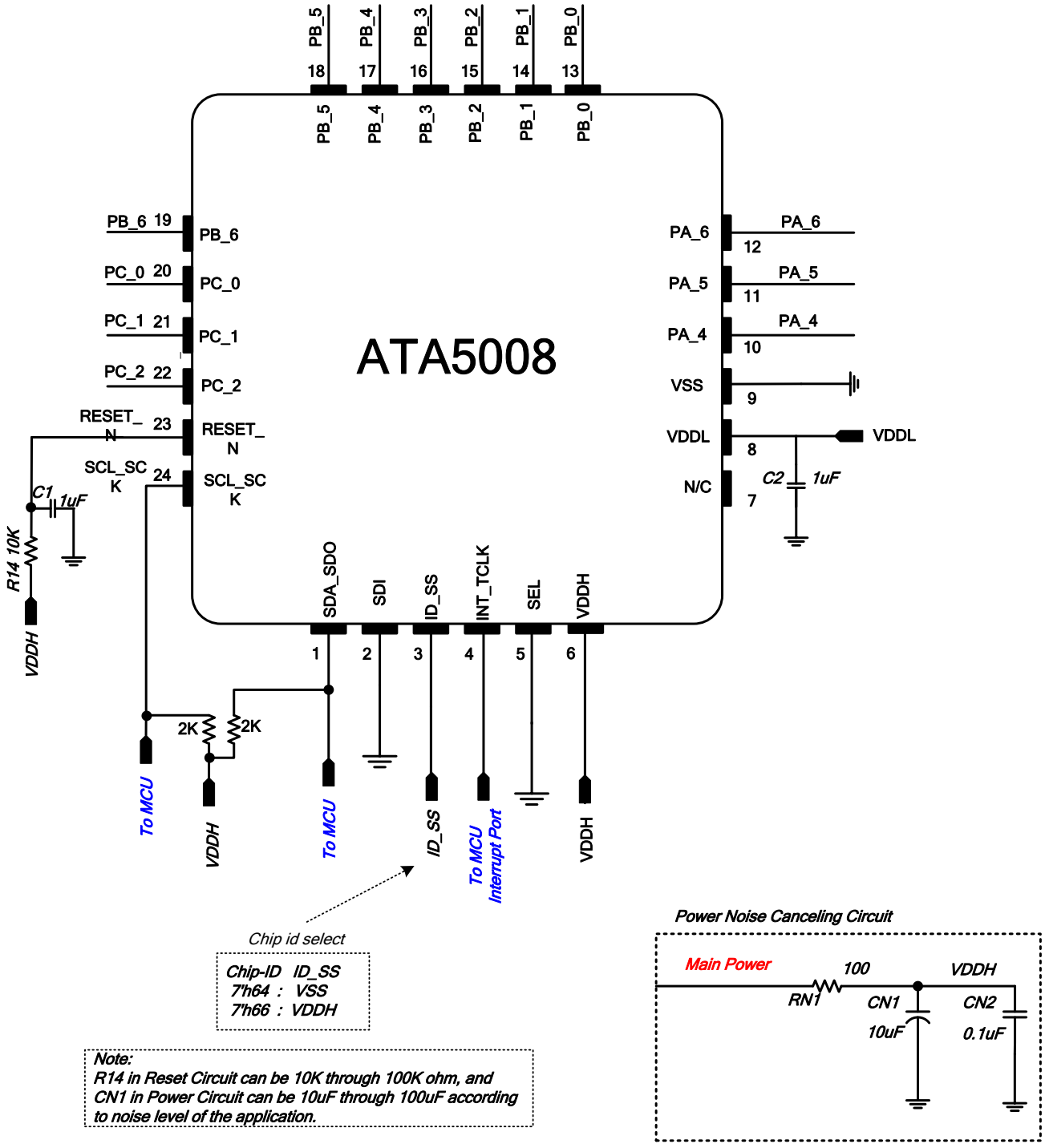
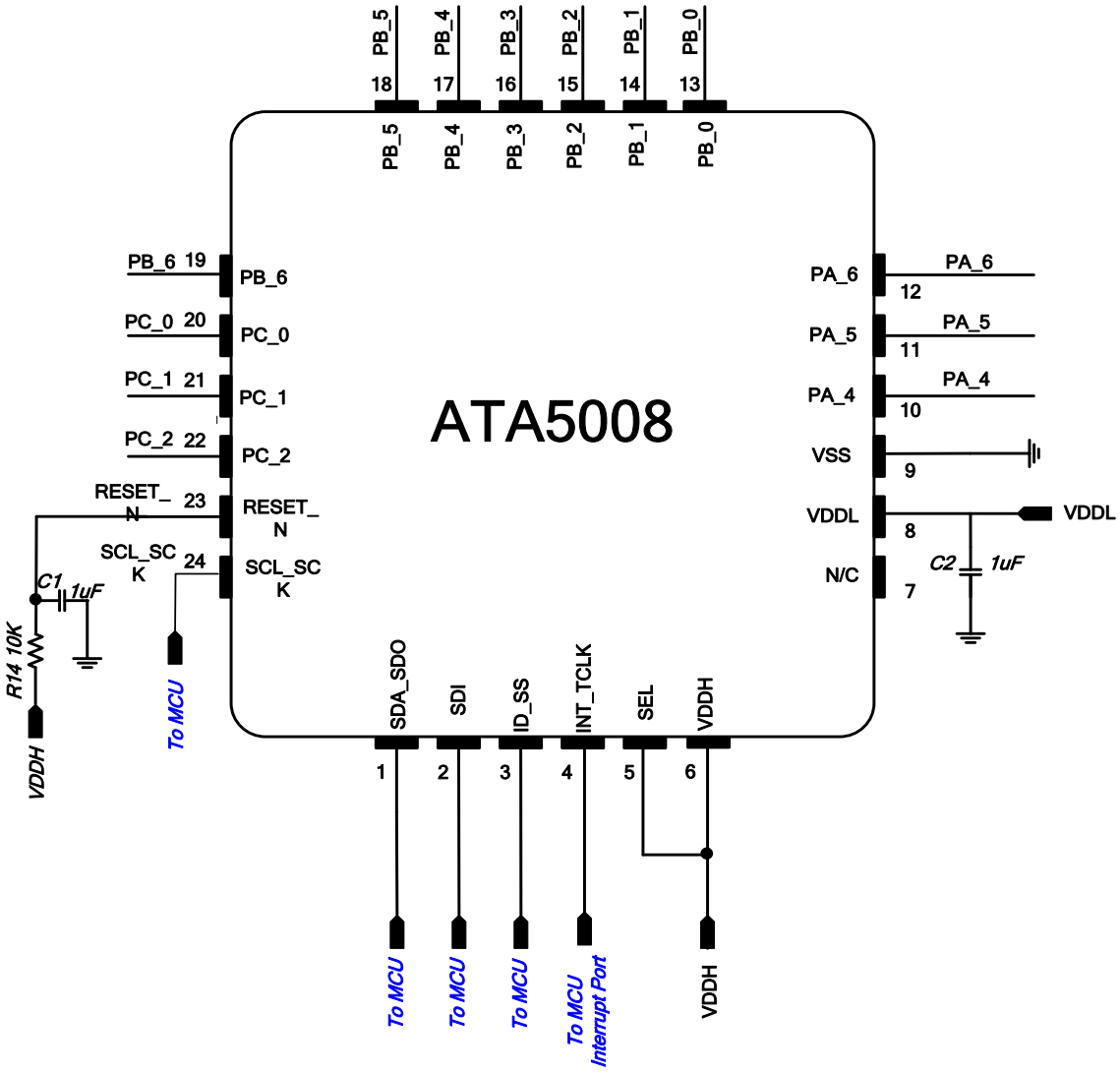
24QFN Application Circuit – I²C Interface

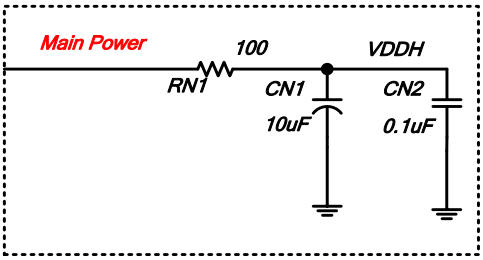


24QFN Application Circuit – SPI Interface



Note:
R14 in Reset Circuit can be 10K through 100K ohm, and CN1 in Power Circuit can be 10uF through 100uF according to noise level of the application.

Power Noise Canceling Circuit



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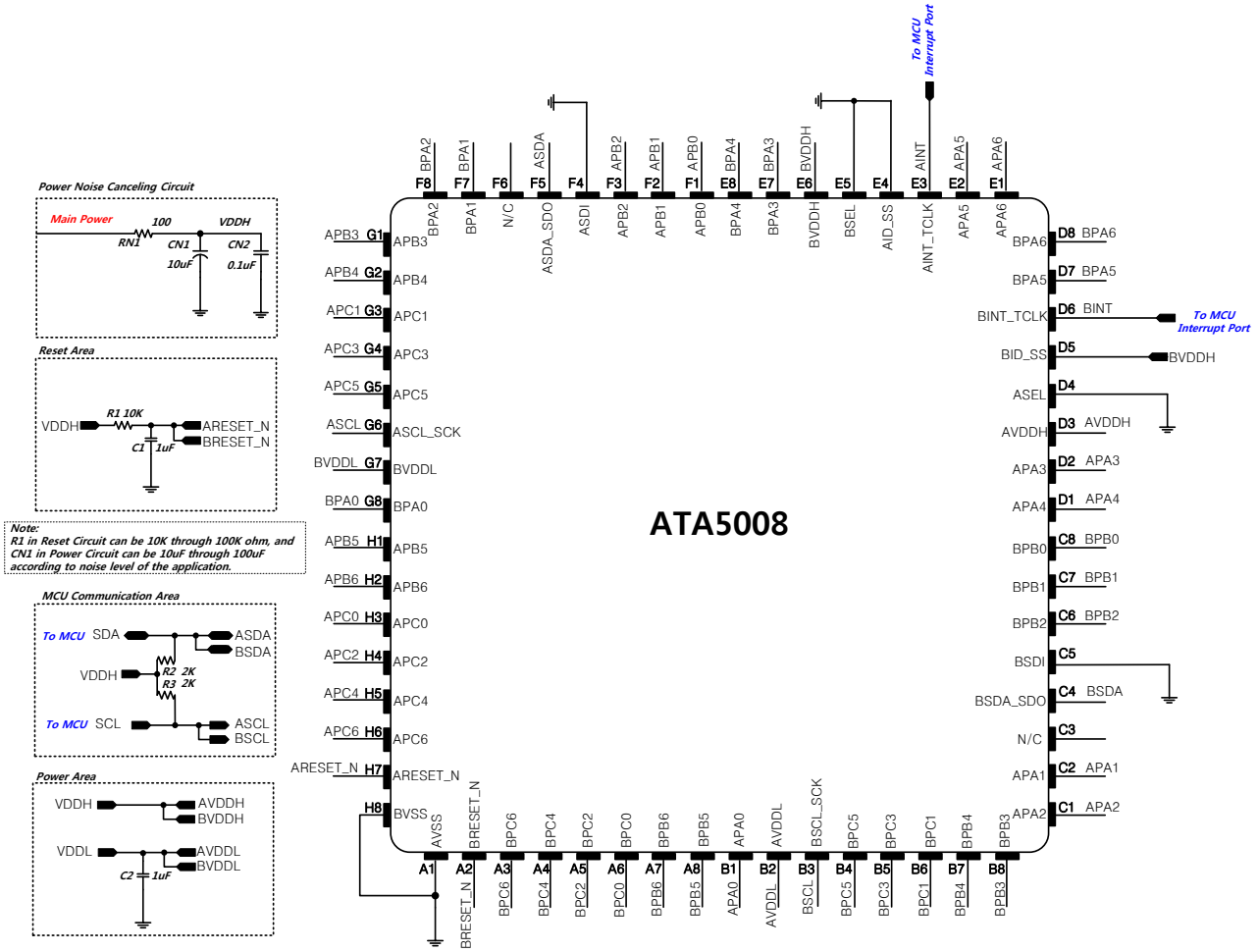
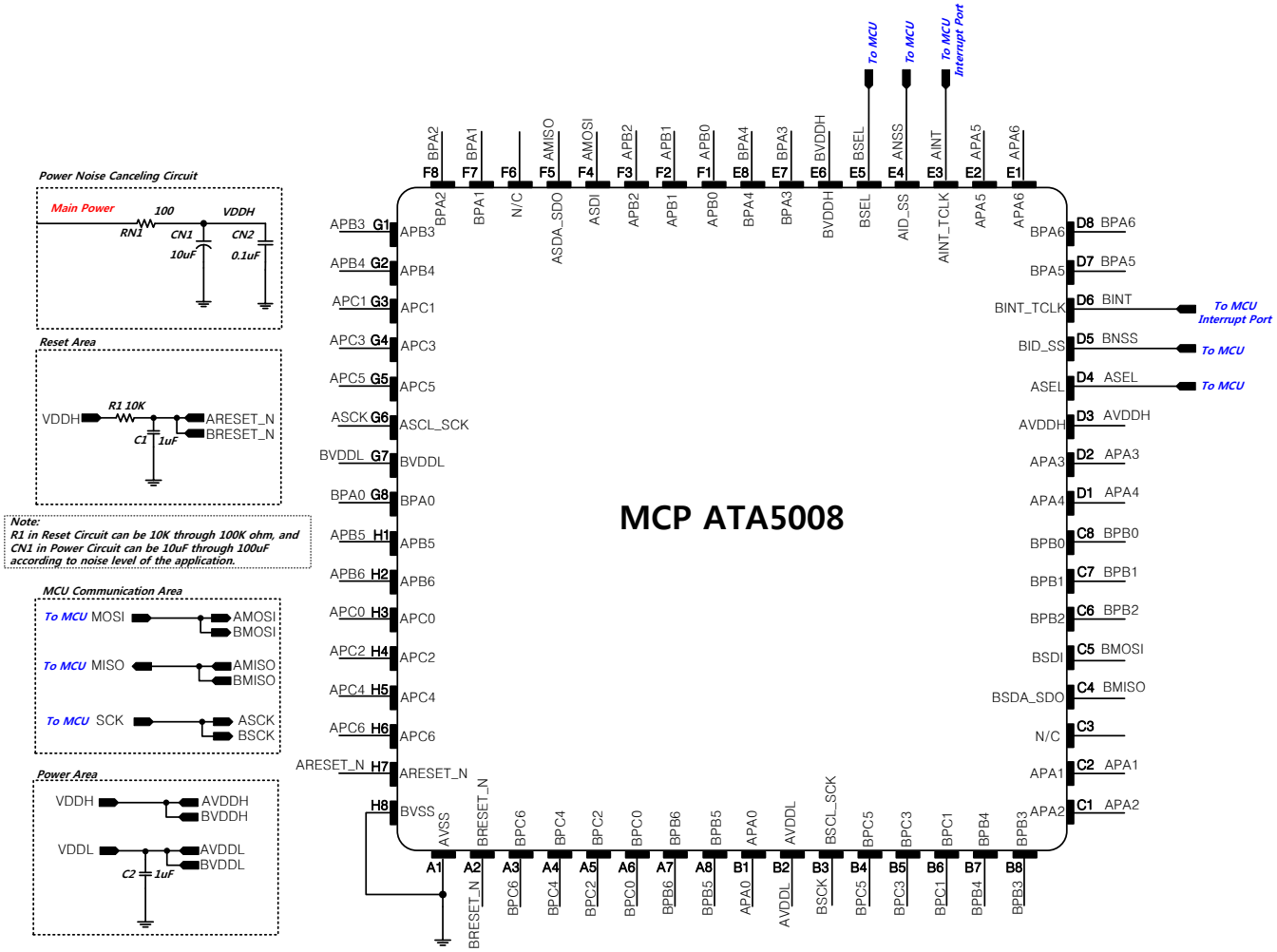
64FBGA Application Circuit – I²C Interface



64FBGA Application Circuit – SPI Interface



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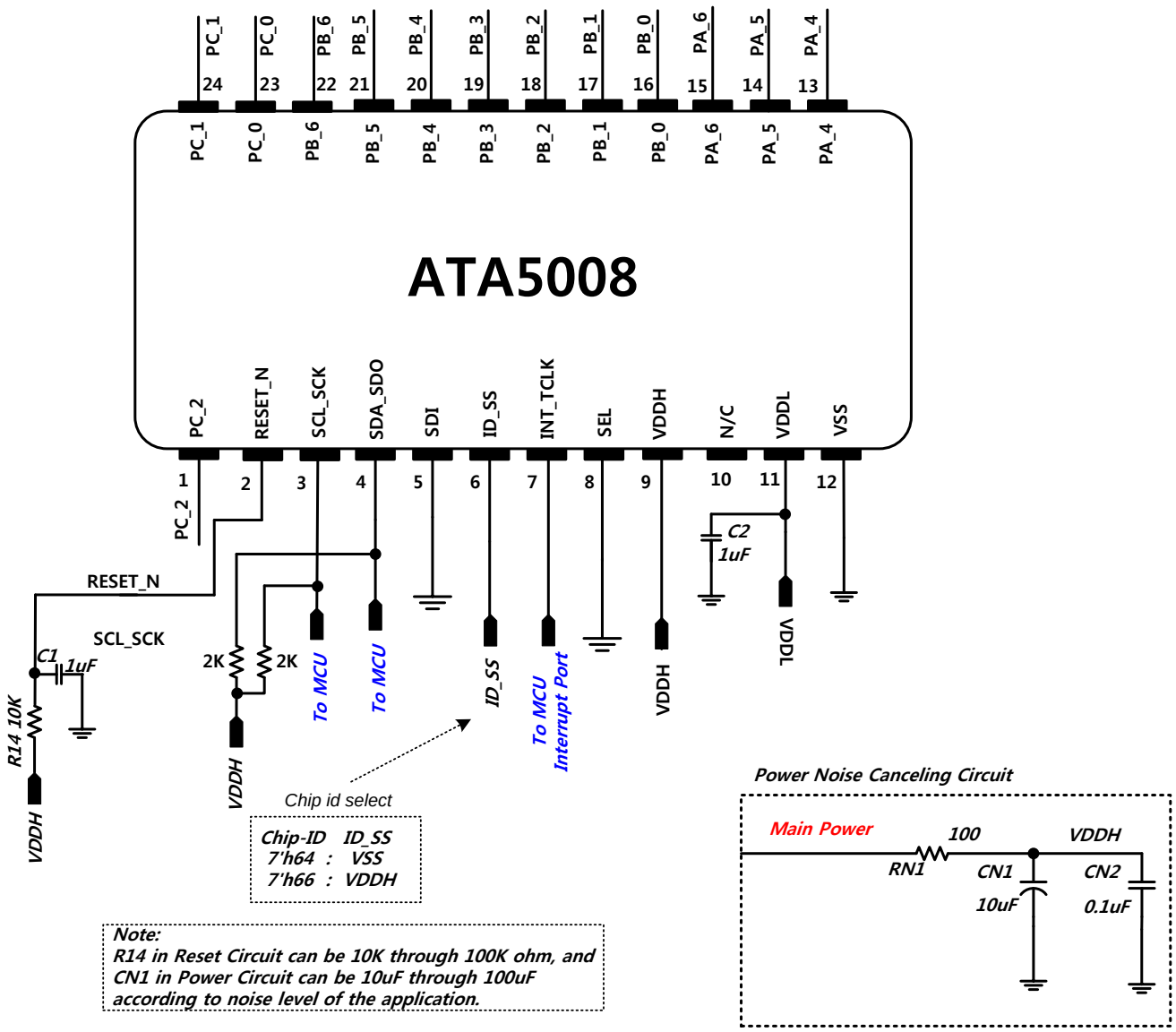
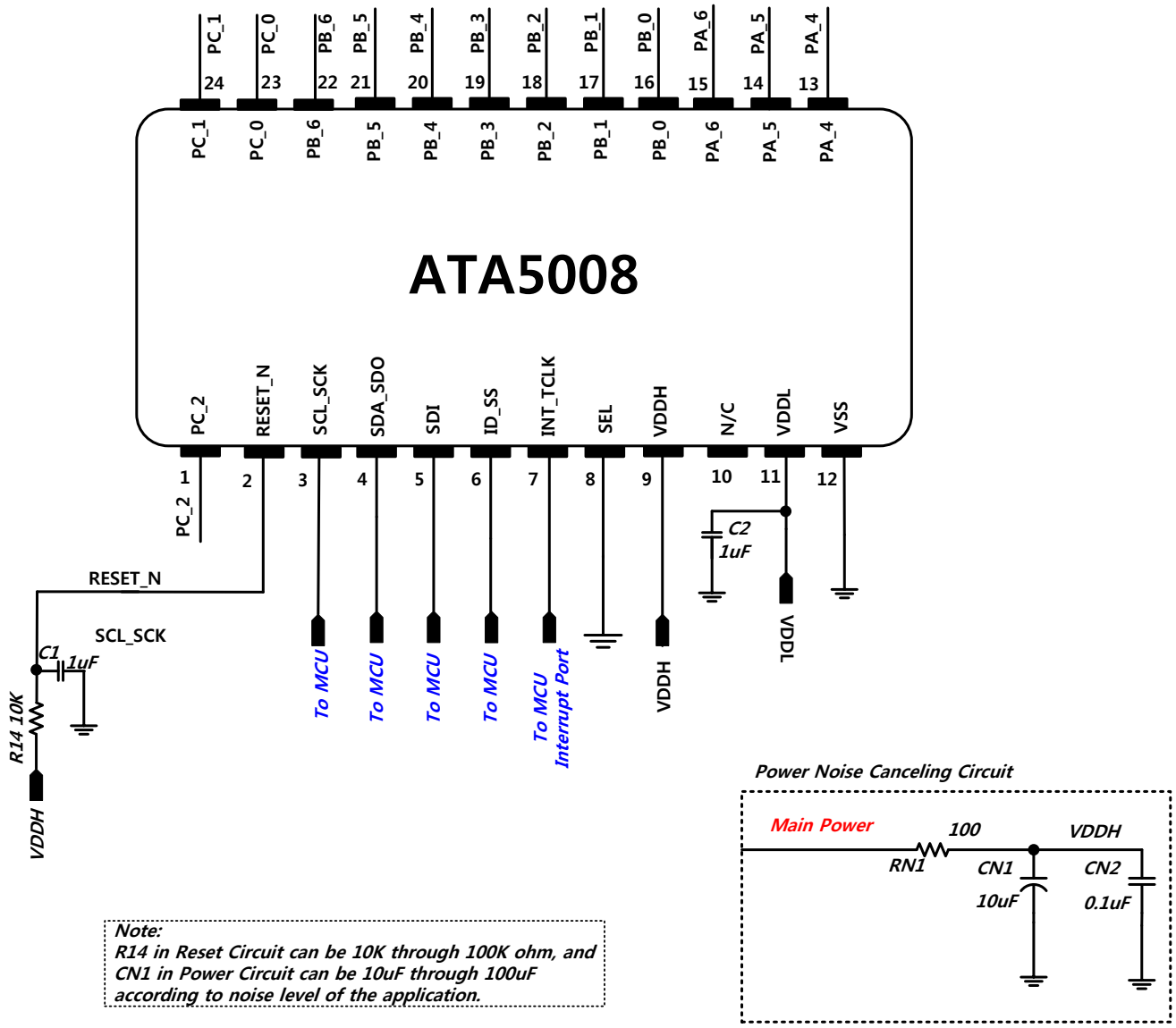
24SSOP Application Circuit – I²C Interface



24SSOP Application Circuit – SPI Interface



Note:
R14 in Reset Circuit can be 10K through 100K ohm, and CN1 in Power Circuit can be 10uF through 100uF according to noise level of the application.

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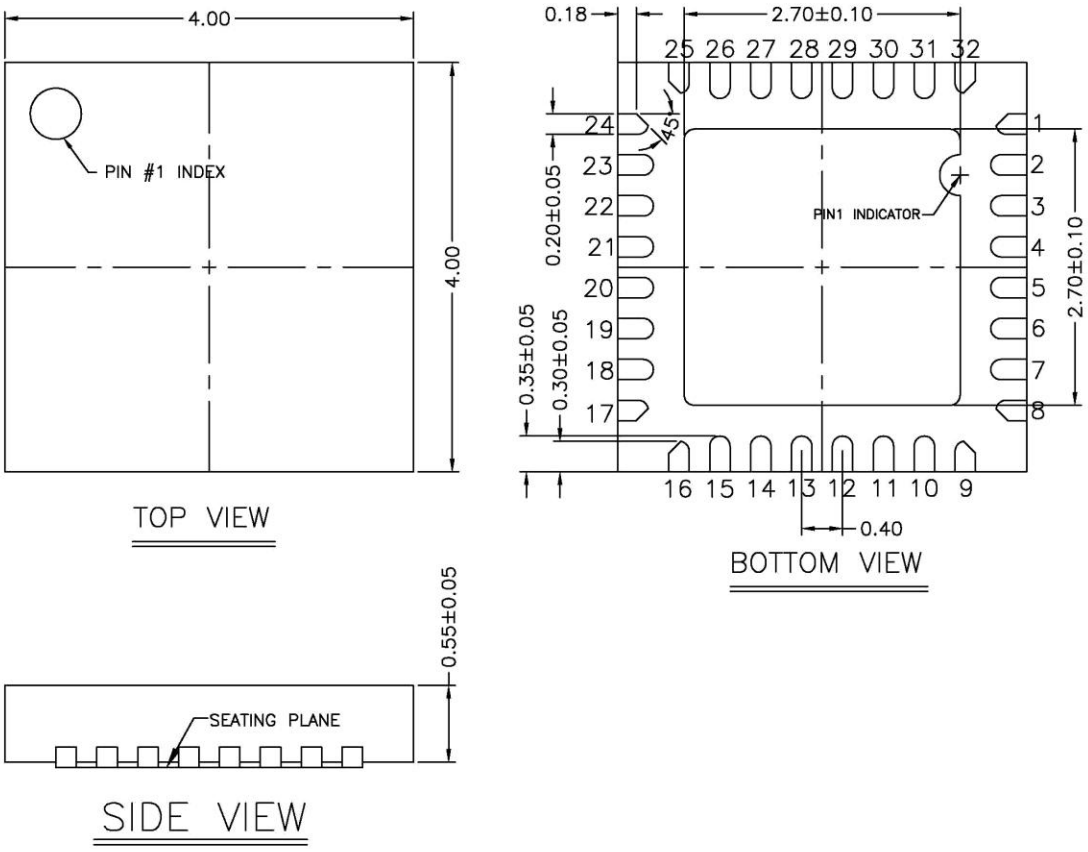
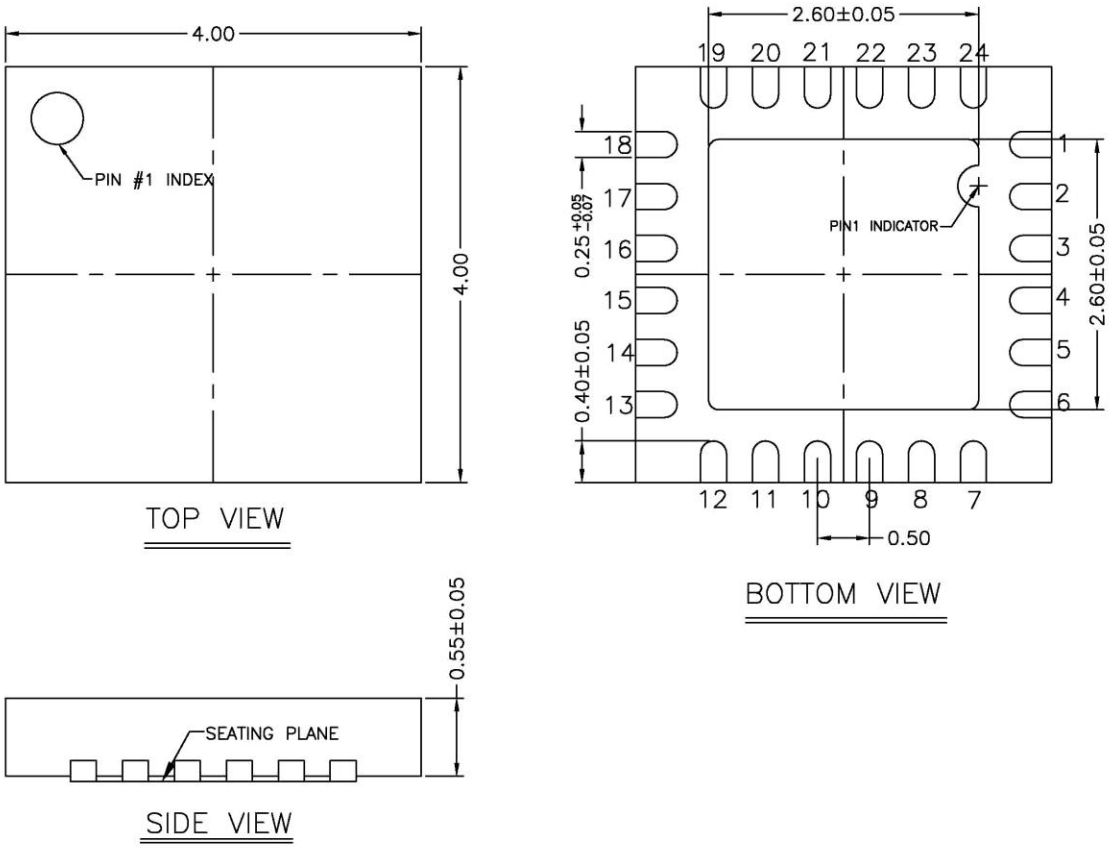
Package Dimensions (Unit: mm)

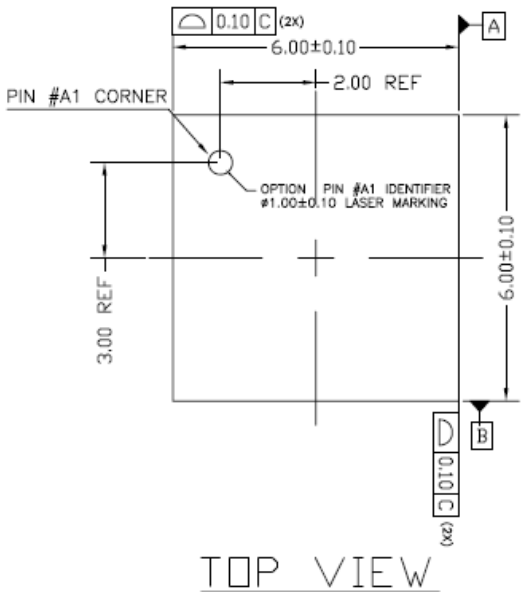
32QFN



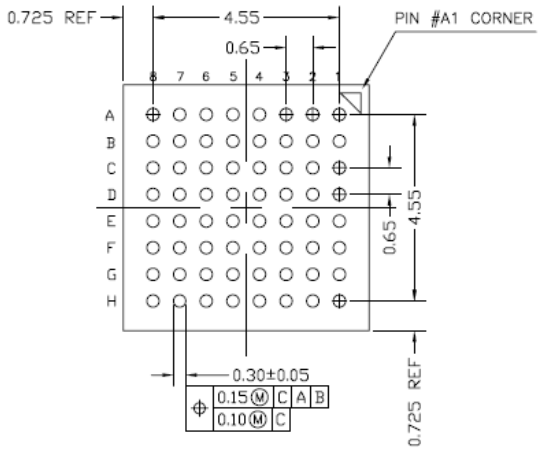
24QFN:


4.00
PIN #1 INDEX
4.00
TOP VIEW
2.60±0.05
19 20 21 22 23 24
18
17
16
15
14
13
1
2
3
4
5
6
12 11 10 9 8 7
0.25 +0.05 -0.07
0.40±0.05
PIN1 INDICATOR
2.60±0.05
0.50
BOTTOM VIEW
0.55±0.05
SEATING PLANE
SIDE VIEW

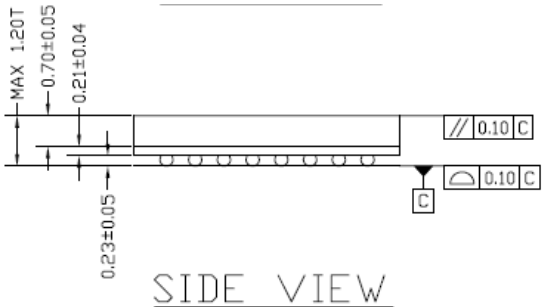
64FBGA



TOP VIEW

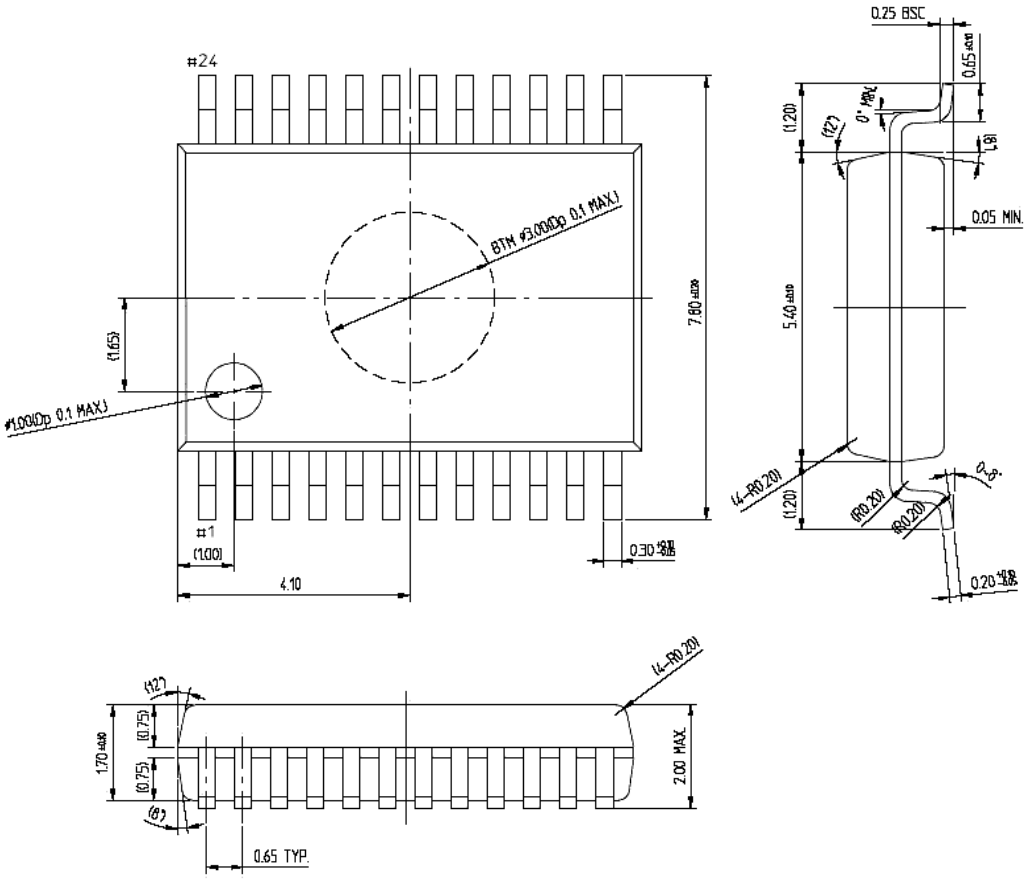


BOTTOM VIEW



SIDE VIEW

24SSOP



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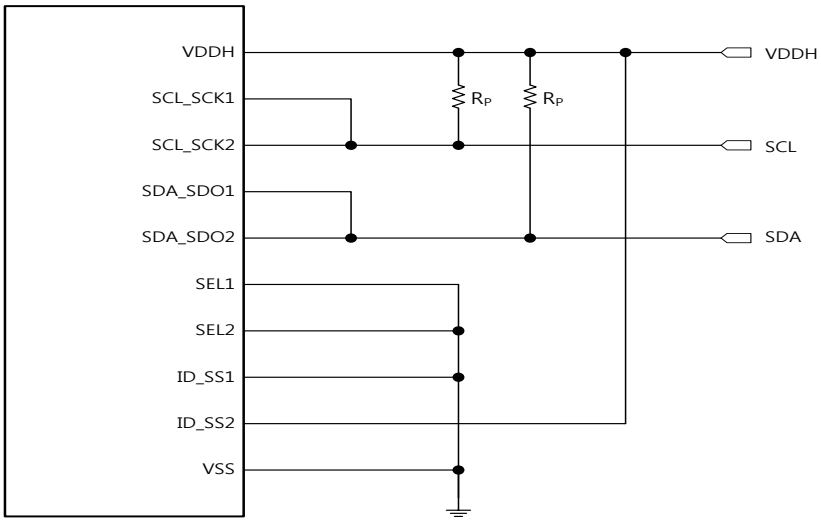
Addendum

64FGBA - I²C Interface

Circuit should be prepared as below for I²C interface. Please refer to ATA5008 User Manual, 'Chapter 6.1 Communication Protocol of I²C Bus' for more detail about I²C Bus Protocol.



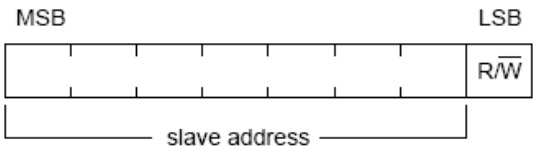
Since ATA5008DA-64B includes two dies of ATA5008 named ATA5008_A and ATA5008_B, two different I2C addresses should be assigned for the access of each device. One is 0x64, and the other is 0x66, respectively.

B6	B5	B4	B3	B2	B1	B0	Hex
1	1	0	0	1	0	0	64

(a)

B6	B5	B4	B3	B2	B1	B0	Hex
1	1	0	0	1	1	0	66

(b)



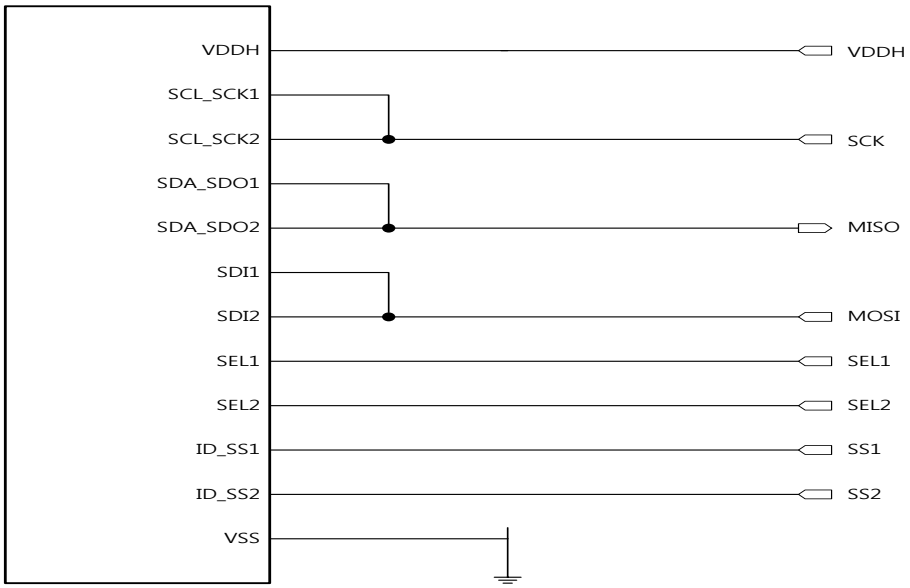
(c)

(a) I²C Address (ATA5008_A), (b) I²C Address (ATA5008_B)

(c) Format of Slave Address with 7 bits

64FBGA - SPI

SPI communication on the ATA500DA-64B supports CPOL=0 and CPHA=0 mode only and works at the clock speed of 500KHz through 2MHz. The circuit of SPI is shown in the figure below. When using two ATA5008 chips or 64FGBA, SEL pin should be controlled by the host as well like SS signal which selects a slave device. For controlling ATA5008_A, SS1, SEL1, SS2 and SEL2 should be low, high, high and low, respectively. Similarly, for controlling ATA5008_B, SS1, SEL1, SS2 and SEL2 should be high, low, low and high, respectively.



SPI packet of 64FGBA consists of 16 bits as shown in the table below.

S	R/W	A/D	Reserved (1 bit)	ADDR or Data (8bits)	Reserved (3Bits)	E

Data Type	Data Width	Description
Start	MOSI[15]	If this bit is '1', then it is a start of the Packet
Read/Write	MOSI[14]	This bit signifies the Read or Write type. 1: Read, 0: Write
Address/Data	MOSI[13]	This bit signifies the next 9 bits are Address or Data. '1': Address, '0': Data.
Reserved	MOSI[12]	This bit should be 0 always.
Address or Data	MOSI[11:4]	These bits signifies Address or Data depending on MOSI[13]

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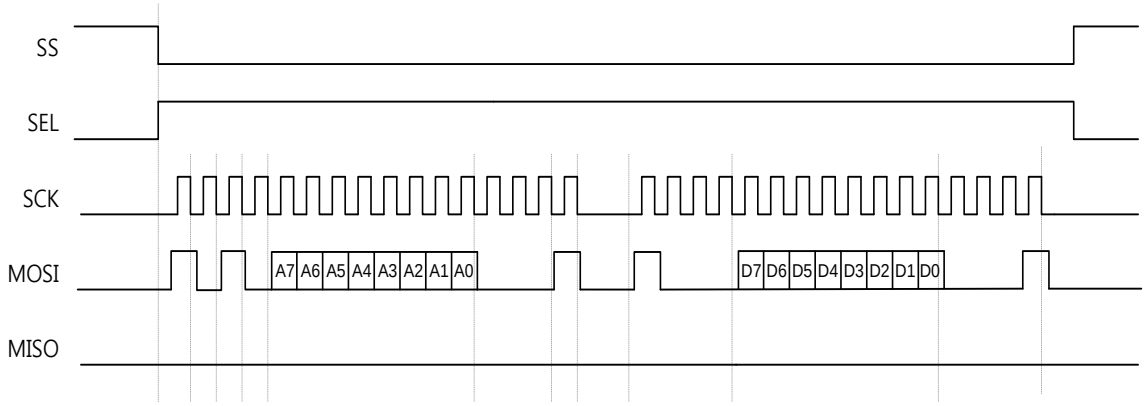
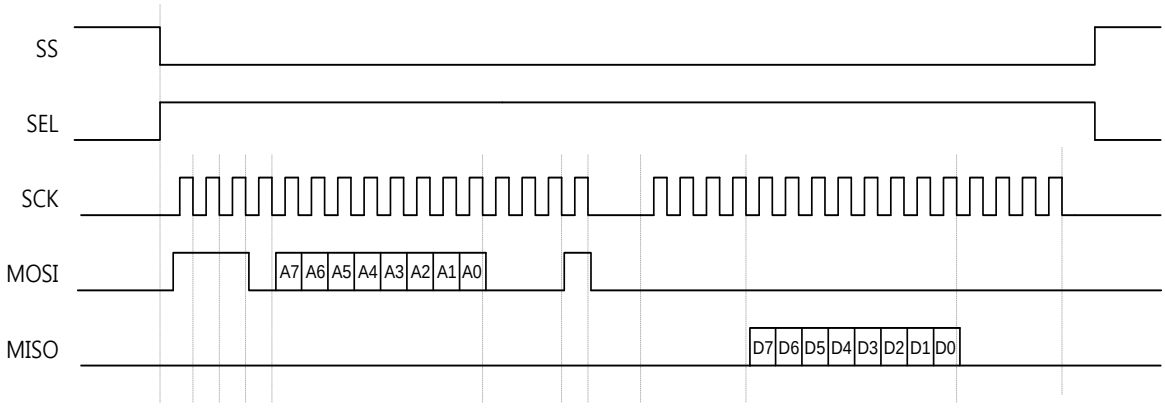
Reserved	MOSI[3:1]	Don't care ('1' or '0')
End	MOSI[0]	For every SPI data transmission this bit should be '1' which signifies the End of the SPI packet. If not, SPI slave (ATA5008) discard the receiving data

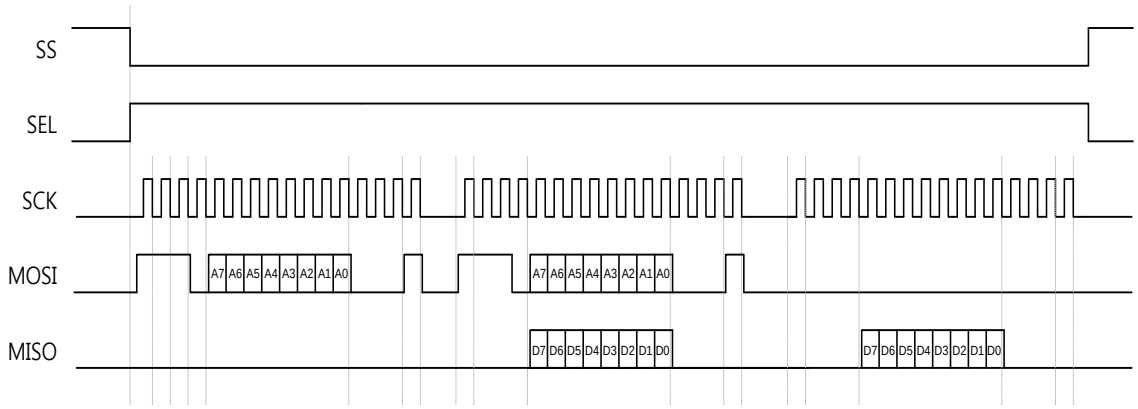
64FBGA supports both Single Read and Burst Read when reading, whereas supports only Single Write when writing. Timing Diagram is shown below.



< SPI Single Write >



< SPI Single Read >



< SPI Burst Read >

Revision History

Date	Revision	Updates
Mar 31, 2009	V0.1	First release
Jun 14, 2009	V0.9	FIFO explanation in Features is deleted Number of APIS modes is changed to two. (APIS mode 1 & 2)
Feb 01, 2010	V1.1	24QFN Pin Description, Application Circuit, Package Dimension
Feb 04, 2010	V1.2	Environmental Specifications, Electrical Specification
Feb 04, 2010	V1.3	Environmental Specifications, Electrical Specification, Vol
Mar 26, 2010	V1.4	Environmental Specifications, Electrical Specification
May 12, 2010	V1.5	Environmental Specifications, Electrical Specification, Application circuit
Jun 10, 2010	V1.6	Features, Environmental Specifications remove.
Aug 10, 2010	V1.7	ATA5008DA-64B added
Aug 11, 2010	V1.8	Ordering Information (32QFN, 24QFN), Package Picture, 64BGA I2C Application Circuit, SPI Single Write Timing Diagram added
Sep 01, 2010	V1.9	32QFN Package Information Updated
Jan 06, 2011	V2.0	24QFN Package Information Updated
Aug 18, 2011	V2.0	24SSOP Package Information Updated

Product Inquiry

In Korea,
ATLab, Inc.
4th Fl, MogAm Bld.
303 BoJeong-Dong GiHeung-Gu, YongIn-Shi
KyungGi-Do 446-770 KOREA
Tel: +82 (31) 266-3082 Fax: +82 (31) 266-3083
Website: http://www.atl21c.com
E-mail: dcc@atlab.co.kr

In China,
ATLab Shenzhen Office
Rm 518-519, Block A, Hailrun Complex 6021 Shenzhen Blvd,
Shenzhen, P.R.C., China Post Code: 518040
Tel: +86 (755) 3333-9445 Fax: +86 (755) 3333-9446

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